n

Is the number of words transferred.

m

Is 1 if bits [32:8] of the multiplier operand are all zero or one.

Is 2 if bits [32:16] of the multiplier operand are all zero or one.

Is 3 if bits [31:24] of the multiplier operand are all zero or one.

Is 4 otherwise.

b

Is the number of cycles spent in the coprocessor busy-wait loop (which can be zero or more).

When the condition is not met, all the instructions take one S-cycle.

Table 7.2. Instruction cycle counts

Instruction	Qualifier	Cycle count
Any unexecuted	Condition codes fail	+S
Data processing	Single-cycle	+S
Data processing	Register-specified shift	+I +S
Data processing	R15 destination	+N +2S
Data processing	R15, register-specified shift	+I +N +2S
MUL	-	+(m)I +S
MLA	-	+I +(m)I +S
MULL	-	+(m)I +I +S
MLAL	-	+I +(m)I +I +S
B, BL	-	+N +2S
LDR	Non-R15 destination	+N +I +S
LDR	R15 destination	+N +I +N +2S
STR	-	+N +N
SWP	-	+N +N +I +S
LDM	Non-R15 destination	+N +(n–1)S +I +S
LDM	R15 destination	+N +(n–1)S +I +N +2S
STM	-	+N +(n–1)S +I +N
MSR, MRS	-	+S
SWI, trap	-	+N +2S
CDP	-	+(b)I +S
MCR	-	+(b)I +C +N
MRC	-	+(b)I +C +I +S
LDC, STC	-	+(b)I +N +(n – 1)S +N

MCR	-	+(b)I +C +N
MRC	-	+(b)I +C +I +S
LDC, STC	-	+(b)I +N +(n – 1)S +N